**REMARKS**

In the Office Action mailed May 5, 2003 the Examiner noted that claims 1-10 are pending, and that claims 1-10 have been rejected. Claims 1-10 have been cancelled, and new claims 11- 26 has been added. No new matter has been added. The Examiner's rejections are traversed below.

**OBJECTION TO DRAWING**

In item 3 on page 2 of the outstanding Office Action, the Examiner stated that FIG. 27 be designated by a legend such as "PRIOR ART". Accordingly, replacement sheet of FIG. 27 is submitted herewith with the heading "PRIOR ART". It is submitted that no new matter has been added.

**REJECTION UNDER 35 U.S.C. § 103(a):**

In the outstanding Office Action, claims 1-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,471,626 ("Carnevale") in view of Applicant's admitted prior art. The rejection is traversed and reconsideration is respectfully requested.

Carnevale discusses a method and apparatus for governing an execution of operations that includes a plurality of large-scale stages in a processor that can be bypassed during an execution. Accordingly, in Carnevale, the governed stages is comprehensive of all the stages in the processor, such as the instruction fetching stage, the write back stage, the address generation stage, etc.

An aspect of the present invention discloses a processor execution pipeline directed to the execution stage of the numerous stages that exist in a processor to reduce the amount of hardware and power consumption required while achieving high-speed processing. Accordingly, "the first and second instructions" are decoded into control signals via "the first and second instruction decoding units" and processed by first and second processing units to be passed to a multiplexer, the value of the stage latch circuits being passed through the bypass line $b_2$ without passing through the processing units. See page 36, lines 6-9, and Abstract of the present invention, and independent claims 11 and 15. Therefore, the value of the stage latch circuits avoids the first and second processing units to pass to the multiplexer. In

contrast, Carnevale is directed to controlling large-stages in the processor by allowing avoidance of different stages during execution. See Carnevale column 1, lines 64-67; FIG. 3 and corresponding text.

Further, in Carnevale, the various stages that correspond to a plurality of data operations executed with respect to data in a processing device can be made variable. See column 4, lines 47-67, and FIG. 3. In Carnevale, even though all control words proceed through the pipeline in the same direction, there are different combinations of stages that the control words may pass through as the control words can enter instruction pipeline at any one of the stages and can also exit the pipeline at any stage. See column 5, lines 5-12; column 1, lines 30-50. However, according to an aspect of the present invention, the processor execution pipeline relates to the execution stage of a process.

According to another aspect of the present invention, stage latch circuits are shared by the execution/operation stages to reduce the amount of hardware and power consumption required in achieving high-speed processing. See page 40, lines 6 through page 41, line 2 in the specification of the present invention, claim 11 and 13. In contrast, Carnevale bypasses the unrelated pipeline stages in which microinstructions progress through in order to reduce the number of machine cycles in which microinstructions reside. See column 1, lines 30-50; column 2, lines 31-45. As such, while Carnevale achieves effective use of available machine cycles, the processor execution pipeline provides sharing of "a latching unit" to reduce the amount of hardware and power consumption in the execution pipeline. For example, according to an aspect of the present invention, it is possible to share the stage latch circuit $110_2$ between the operator $120_1$ and the operator $120_2$. See page 40, line 22-25 in the specification of the present invention.

The burden of establishing a prima facie case of obviousness based upon the prior art lies with the Examiner. In re Fritch, 23 U.S.P.Q. 2d 1780, 1783 (Fed. Cir. 1992). According to In re Fritch, the Examiner "... can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." Carnevale does not teach a processor execution pipeline directed to the execution stage out of the numerous stages that exist in a processor to reduce the amount of hardware and power consumption required while achieving high-speed processing.

The Examiner correctly stated that Carnevale does not explicitly teach "a first and

second processing units provided at the first and second processing stages" that process instructions by processing data held in the latching units. The Examiner also stated that Carnevale teaches each pipeline stage executes particular operation related to a certain purpose and control words. As emphasized by the following amendment to the claims, the different aspects of the present invention are mainly directed to the execution stage in a processor and not other preceding and subsequent stages in the process. Accordingly, withdrawal of the rejection is requested.

**NEW CLAIMS**

New claims 11 through 26 have been added to clarify that the present invention is mainly directed to the execution stage of the various stages in a processor. Further, unlike Carnevale, high speed processing is achieved according to an aspect of the present invention by allowing stage latch circuits to be shared. As recited in dependent claim 13, "a latching unit holds the output of the first processing unit where the second data is data held by the latching unit". Specifically, the latching unit holds both the first data, which is output by the first processing unit, and second data, accessed by the second processing unit, allowing first and second processing units to share the stage latch circuit. See dependent claim 13, and independent claim 1.

Therefore, Carnevale does not teach or suggest each of the features of independent claims 11, 15, 19, and 23. Thus, withdrawal of the rejection is requested.

**CONCLUSION**

In accordance with the foregoing amendments and remarks, it is submitted that claims 11-26 patentably distinguish over the references cited by the Examiner. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8(a)
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
on September 8, 2003
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PRIOR ART





FIG.27